dc-304666°FORM PTO-1390 (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
449122023600	10/070535 Not yet assigned

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/03086	September 6, 2000	September 7,1999

TITLE OF INVENTION

METHOD AND APPARATUS FOR INTERCHANGING DATA BETWEEN MODULES CONNECTED TO A COMMON BUS (AS AMENDED)

APPLICANT(S) FOR DO/EO/US

Franz HUTNER et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application under PCT Article 19 (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☒ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items: 1) Application Data Sheet; 2) Int'l Search Report; 3) IPER; 4) Return receipt postcard.

CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on March 7, 2002.

Melissa Garton

Melissa Garton

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY DOCKET NO.
Not yet assigned 10/070535	PCT/DE00/03086	449122023600

21. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1,040.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $890.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $740.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provision of PCT Article 33(1)-(4) $710.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00

	CALCULATIONS PTO USE ONLY	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$0	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	- 20 =		x $18.00	$0	
Independent claims	- 3 =		x $84.00	$0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $280.00	$0	
			TOTAL OF ABOVE CALCULATIONS =	$890.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.				$0	
			SUBTOTAL =	$890.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).			+	$0	
			TOTAL NATIONAL FEE =	$890.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00 per property**			+	$40.00	
			TOTAL FEES ENCLOSED =	$930.00	
				Amount to be refunded:	**$**
				charged:	**$**

a. ☒ Please charge my **Deposit Account No. 03-1952** (referencing Docket No. 449122023600) in the amount of $930.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

b. ☒ The Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment to **Deposit Account No. 03-1952** (referencing Docket No. 449122023600).

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Kevin R. Spivak
Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
Washington, D.C. 20006-1888

SIGNATURE

Kevin R. Spivak
Registration No. 43,148

March 7, 2002

CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on March 7, 2002.

Melissa Garton

Melissa Garton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Franz HUTNER et al.

Serial No.: Not yet assigned

Filing Date: March 7, 2002

For: METHOD AND APPARATUS FOR INTERCHANGING DATA BETWEEN MODULES CONNECTED TO A COMMON BUS *(AS AMENDED)*

Examiner: Not yet assigned

Group Art Unit: Not yet assigned

PRELIMINARY AMENDMENT

BOX PCT
Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination on the merits, please amend this application as follows:

In the Specification:

Please amend the Title as follows:

METHOD AND APPARATUS FOR INTERCHANGING DATA BETWEEN MODULES CONNECTED TO A COMMON BUS

In the Claims:

Please cancel claims 1-9.

Please add the following new claims 10-18:

What is claimed is:

10. (New) A method for interchanging data between modules connected to a common bus, comprising:

synchronizing a plurality of modules in time;

outputting bus request information from one of the plurality of modules to the other modules; and

storing a clock cycle of the output in each of the modules and an origin of the bus request information in a request memory, wherein

each module uses the stored bus request information to independently determine whether there is a signal on the bus in a particular clock cycle, the decision being made on the basis of a prescribed decision pattern which is identical for each of the modules.

11. (New) The method as claimed in claim 1, wherein at the start of the method, resetting the request memories into an identical initial.

12. (New) The method as claimed in claim 1, wherein on the basis of the decision pattern, the bus is operated by the plurality of modules in the order in time in which the corresponding bus request information was output.

13. (New) The method as claimed in claim 3, wherein if the plurality of modules output bus request information at the same time in a clock cycle, the corresponding information is stored in a shared memory block in the request memory, and the bus is used in a prescribed order on the basis of information stored in a memory block.

14. (New) The method as claimed in claim 4, wherein the plurality of modules output no additional bus request information if the number of the at least partly used memory blocks has reached a prescribed limit value.

15. (New) The method as claimed in claim 1, wherein at least one of the modules outputs bus request information having a higher priority level, and the information is stored in a second memory, the bus is used on the basis of a prescribed use algorithm for bus request information in

the request memory or for bus request information having the higher priority level in the second memory, and the bus is used on the basis of the bus request information having the higher priority level irrespective of use on the basis of the normal bus request information.

16. (New) A system for interchanging data between modules connected to a common bus, comprising:

request lines, which respectively connect one module to the other modules, to transmit bus request information;

a request memory in each of the modules to store a clock cycle of an output and an origin of the bus request information;

a bus use circuit in each of the modules to control bus use by a respective module on the basis of the bus request information stored in the request memory in line with a decision pattern which is prescribed and identical for the modules; and

a timer line, connected to the modules, to synchronize the modules.

17. (New) The system as claimed in claim 7, further comprising a line to transmit a reset signal which puts the request memories into a standard initial state.

18. (New) The system as claimed in claim 7, wherein each module has another memory for higher priority bus request information which is output by at least one of the modules, the bus use circuits taking into account the higher priority bus request information stored in the another memory on the basis of a prescribed use algorithm.

In the Abstract:

Please replace the Abstract with the substitute Abstract attached hereto.

REMARKS

Amendments to the specification have been made and are submitted herewith in the attached Substitute Specification. We have included both a clean copy of the specification and a marked-up version showing the changes made. The claims and abstract have been amended herewith in the Preliminary Amendment. All amendments have been made to place the application in proper U.S. format and to conform with proper grammatical and idiomatic English. None of the amendments herein are made for reasons related to patentability. No new matter has been added.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**".

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 449122023600. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Respectfully submitted,

Dated: March 7, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

For the convenience of the Examiner, the changes made are shown below with deleted text in strikethrough and added text in underline.

In the Specification:

Please amend the Title as follows:

METHOD AND APPARATUS FOR INTERCHANGING DATA BETWEEN MODULES CONNECTED TO A COMMON BUS

In the Claims:

Please cancel claims 1-9.

Please add the following new claims 10-18:

~~Patent Claims~~

What is claimed is:

10. (New) A method for interchanging data between modules connected to a common bus, comprising:

synchronizing a plurality of modules in time;

outputting bus request information from one of the plurality of modules to the other modules; and

storing a clock cycle of the output in each of the modules and an origin of the bus request information in a request memory, wherein

each module uses the stored bus request information to independently determine whether there is a signal on the bus in a particular clock cycle, the decision being made on the basis of a prescribed decision pattern which is identical for each of the modules.

11. (New) The method as claimed in claim 1, wherein at the start of the method, resetting the request memories into an identical initial.

12. (New) The method as claimed in claim 1, wherein on the basis of the decision pattern, the bus is operated by the plurality of modules in the order in time in which the corresponding bus request information was output.

13. (New) The method as claimed in claim 3, wherein if the plurality of modules output bus request information at the same time in a clock cycle, the corresponding information is stored in a shared memory block in the request memory, and the bus is used in a prescribed order on the basis of information stored in a memory block.

14. (New) The method as claimed in claim 4, wherein the plurality of modules output no additional bus request information if the number of the at least partly used memory blocks has reached a prescribed limit value.

15. (New) The method as claimed in claim 1, wherein at least one of the modules outputs bus request information having a higher priority level, and the information is stored in a second memory, the bus is used on the basis of a prescribed use algorithm for bus request information in the request memory or for bus request information having the higher priority level in the second memory, and the bus is used on the basis of the bus request information having the higher priority level irrespective of use on the basis of the normal bus request information.

16. (New) A system for interchanging data between modules connected to a common bus, comprising:

request lines, which respectively connect one module to the other modules, to transmit bus request information;

a request memory in each of the modules to store a clock cycle of an output and an origin of the bus request information;

a bus use circuit in each of the modules to control bus use by a respective module on the basis of the bus request information stored in the request memory in line with a decision pattern which is prescribed and identical for the modules; and

a timer line, connected to the modules, to synchronize the modules.

17. (New) The system as claimed in claim 7, further comprising a line to transmit a reset signal which puts the request memories into a standard initial state.

18. (New) The system as claimed in claim 7, wherein each module has another memory for higher priority bus request information which is output by at least one of the modules, the bus use circuits taking into account the higher priority bus request information stored in the another memory on the basis of a prescribed use algorithm.

In the Abstract:

Please replace the Abstract with the substitute Abstract attached hereto.

METHOD AND APPARATUS FOR INTERCHANGING DATA BETWEEN MODULES CONNECTED TO A COMMON BUS

Abstract

In a method for interchanging data between modules connected to a common bus, all the modules are synchronized. A module wishing to operate the bus outputs bus request information which is received and stored by the modules. Each module uses the stored bus request information to decide, independently of the others, whether there is a signal on the bus in a particular clock cycle, the decision being made on the basis of a prescribed decision pattern which is identical for all the modules.

METHOD AND APPARATUS FOR INTERCHANGING DATA BETWEEN MODULES CONNECTED TO A COMMON BUS

CLAIM FOR PRIORITY

This application claims priority to International Application No. PCT/DE00/03086 which was published in the German language on September 6, 2000.

TECHNICAL FIELD OF THE INVENTION

The present invention relates to a method and apparstus for interchanging data between modules connected to a common bus.

BACKGROUND OF THE INVENTION

Conventionally, computers contain a series of hardware modules which are connected to a common bus, for example to an ISA bus or to a PCI bus. In this context, a plurality of these hardware modules - generally called bus masters - are authorized to send to the bus lines signals which can then be received by the other bus users, e.g. slaves. In this case, it is necessary to ensure that two bus masters do not send signals to the bus lines at the same time. For this reason, the bus systems normally have a central administration module (arbiter) which allocates the bus to the individual bus masters at particular times for data transmission.

If a bus master wants to use the bus for a particular period of time, it sends the arbiter appropriate bus request information via a request line connecting the bus master to the central arbiter. In this context, one request line needs to be provided between every single bus master and the arbiter. The arbiter itself has, by way of example, a memory storing the bus requests coming from the various bus masters, and then allocates the bus to one of the bus masters for one or more clock cycles on the basis of a prescribed decision pattern. In this context, the bus is allocated by transmitting a special grant signal via an allocation or grant line, and again there needs to

be one such grant line between every single bus master and the arbiter.

Since the individual bus masters respectively output data to the bus only when they have been granted permission to do so by the central arbiter, two bus masters are certain never to operate the bus, i.e. to send a signal to the bus lines, at the same time.

If the bus system is very large, highly ramified and has a very large number of bus users, then the solution described above often needs to allow for a relatively long delay time for the request and allocation information. However, this means that the bus can operate only at a relatively low clock rate and hence slowly on the whole. Another problem is that, although the bus masters can at any time send their bus request information to the arbiter, they need to wait for some time until they can actually use the bus. However, since the exact time of bus allocation is not known, the time between sending the bus request information and receiving the allocation information remains unused. The result of this is that the individual bus users cannot utilize their computation power to optimum effect.

SUMMARY OF THE INVENTION

In one embodiment of the invention, there is a method for interchanging data between modules connected to a common bus. The method includes, for example, synchronizing a plurality of modules in time, outputting bus request information from one of the plurality of modules to the other modules, and storing a clock cycle of the output in each of the modules and an origin of the bus request information in a request memory, wherein each module uses the stored bus request information to independently determine whether there is a signal on the bus in a particular clock cycle, the decision being made on the basis of a prescribed

decision pattern which is identical for each of the modules.

In another aspect of the invention, at the start of the method, resetting the request memories into an identical initial.

In another aspect of the invention, on the basis of the decision pattern, the bus is operated by the plurality of modules in the order in time in which the corresponding bus request information was output.

In yet another aspect of the invention, if the plurality of modules output bus request information at the same time in a clock cycle, the corresponding information is stored in a shared memory block in the request memory, and the bus is used in a prescribed order on the basis of information stored in a memory block.

In another aspect of the invention, the plurality of modules output no additional bus request information if the number of the at least partly used memory blocks has reached a prescribed limit value.

In another aspect of the invention, at least one of the modules outputs bus request information having a higher priority level, and the information is stored in a second memory, the bus is used on the basis of a prescribed use algorithm for bus request information in the request memory or for bus request information having the higher priority level in the second memory, and the bus is used on the basis of the bus request information having the higher priority level irrespective of use on the basis of the normal bus request information.

In another embodiment of the invention, there is a system for interchanging data between modules connected to a common bus. The system includes, for example, request lines, which respectively connect one module to the other modules, to transmit bus request information, a request memory in each of the modules to store a

clock cycle of an output and an origin of the bus request information, a bus use circuit in each of the modules to control bus use by a respective module on the basis of the bus request information stored in the request memory in line with a decision pattern which is prescribed and identical for the modules, and a timer line, connected to the modules, to synchronize the modules.

In another aspect of the invention, the system includes a line to transmit a reset signal which puts the request memories into a standard initial state.

In another aspect of the invention, each module has another memory for higher priority bus request information which is output by at least one of the modules, the bus use circuits taking into account the higher priority bus request information stored in the another memory on the basis of a prescribed use algorithm.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is explained in more detail below with reference to the appended drawings, in which:

Figure 1 shows an illustration of the inventive linking of four bus users.

Figure 2 shows a storage and processing of bus request information.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention specifies a method and a system for interchanging data between modules connected to a common bus where the bus lines and the computation capacities of the individual modules can be used as effectively as possible.

According to one embodiment of the invention, the bus system is not administered by a single central administration module, but rather by all the modules incorporated in the system. Each module deciding, independently of the other bus users, whether it sends data to the bus lines during a particular bus clock

cycle. Hence, each module has a personal arbiter of its own. So that this method also ensures that the bus is not operated by two users at the same time during a particular clock cycle, a module requesting use of the bus first outputs bus request information which is received by all the other modules. The time of the request - e.g. the clock cycle - and the origin of the bus request information - for example a number or address for the module - are stored in a request memory which is present in the modules (including in the request memory in that module which has itself output the bus request information), so that the modules have the same bus request information available. On the basis of this bus request information, the modules then decide, in each case individually, whether they use the bus in a particular clock cycle, the decision being made on the basis of a prescribed decision pattern which is identical for the modules.

Since each bus user decides directly whether it uses the bus, this method eliminates the delay time for the allocation or grant signal, which means that the bus can operate more quickly on the whole. Since the bus users now have identical bus arbiters, i.e. arbiters which store the bus request information in the same way and make a decision about the bus use on the basis of the identical decision pattern, each bus user knows the current use status and the subsequent use status of the bus. An individual module, for example which knows that it cannot use the bus for a few clock cycles, can use the time in between for other tasks, which means that the inventive method allows more effective utilization of the individual bus users. So that the distributed arbiters can operate starting form the same basic state, they are synchronized at the start using a synchronous reset signal.

Preferably, the decision about use of the bus is made on the basis of the decision pattern such that the bus is operated by the modules in the order in time in which the bus request information was output. In this case, the request memories present in the bus users are

preferably in the form of a FIFO (First in, First out). Normally, however, the smallest unit of time which can still be distinguished in bus systems is a single clock cycle. It is therefore possible for a plurality of modules to output bus request information at the same time in a clock cycle. Provision can then be made for the order of bus use to be produced by a plurality of bus request information items output in a single clock cycle on the basis of a specific prescribed order.

The smallest unit of time which can still be distinguished in the bus system is a single clock cycle, as mentioned previously. The case may therefore arise in which a plurality of modules (in the extreme case all of the modules) make a request in one clock cycle, in which case one respective module can use the actual bus lines used for transmitting signals per clock cycle. If, for example in a system in which a bus transfer uses the bus for one clock cycle, n bus users request the bus at the same time, then the entire processing or use of the bus takes n clock cycles on account of these n requests, whereas the requests were themselves output in a single clock cycle. This in turn means that, while the n requests are being processed, the bus users can continue to make new requests, so that the request memory can become full over time. To prevent requests from being made which are no longer stored and hence can also no longer be processed, it is necessary to ensure that each module "knows" when the memory resources for new requests have been exhausted. Since the local arbiters in each module are of identical design, and hence the utilization of the memory resources is the same everywhere, each individual module can obtain or derive this information from its personal arbiter, so that it is possible to stipulate that the modules send no further requests to their request lines until memory capacity is free again in their own arbiter.

In another embodiment, some of the bus users perform more important tasks for the overall system, which means that their bus requests should be handled

with preference. Provisions can be made for each bus user to have, besides the original request memory, a further request memory for requests having a higher priority level, in which the requests from these special bus users are stored separately. On the basis of the decision pattern, provisions can then be made for the bus to be used on the basis of a prescribed sequence for requests from the normal request memory or for requests having the higher priority level. This second request memory is filled, and the order in time of the bus use by the prioritized requests occurs, irrespective of the processing of the normal bus requests. If further different priority levels need to be taken into account as well, then a correspondingly large number of request memories are required and the arbitration algorithm, that is to say the order in which the bus is used by requests from the various memories, needs to be adjusted as appropriate.

In another aspect of the invention, a bus system for interchanging signals between a plurality of modules is specified where each module has an outgoing request line which branches to the other modules, and where each module has at least one request memory storing the time of bus request information and the origin thereof, and also a bus use circuit which, on the basis of the stored bus request information, permits or prevents use of the bus by the module in a particular clock cycle in line with a prescribed decision pattern which is identical for the modules.

In this context, the term module denotes every single bus user, which can involve combined assemblies or else single IC chips, for example.

Figure 1 shows the connection of four modules 1-4 in an inventive bus system. It does not show the bus lines used for the actual data transfer. Each module 1-4 has a respective outgoing request line R1-R4 which branches to the other modules, so that bus request information can be communicated to the modules. To allow the modules 1-4 to respond synchronously in time, they are synchronized by a common timer line C1. In

addition, a reset signal can be transmitted to the modules 1-4 at the start via a reset line Re, the reset signal putting the bus users, specifically the respective arbiters - e.g. the bus use circuits - and the content of the request memories, into a common initial state. According to the invention, any of the modules 1-4 makes a bus request for use of the bus for the duration of a transfer by activating its respective request line R1-R4 for one clock cycle. If the module wishes to request the bus for two transfers, the appropriate request line R1-R4 is activated for two clock cycles.

The filling of the request memory and the processing of the various requests will now be explained with reference to figure 2. Figure 2 shows the first module 1 in enlarged form. The arbiter A1 (the bus use circuit) responsible for use of the bus lines has in this case been permanently incorporated into the module 1. In addition, this arbiter A1 first has an associated first request memory 5, which is preferably in the form of a FIFO.

In the present example, it may first be assumed that a total of four modules are available as bus users with equal authorization. The module 1 makes a bus use request by activating its internal request line 7. This internal request line 7 is connected first directly to the request memory 5 and secondly to the external request line R1, which in turn branches to the other modules - as shown in the present case to the second module 2.

Since the delay times for the bus request information can vary slightly depending on the length of the request lines R1-R4, the information regarding in which clock cycle a request was made is stored in the request memory 5, but not the exact time. Within a clock cycle, each module 1-4 can make a maximum of one requests. This is covered by virtue of all the requests made within a clock cycle being stored in a memory block, corresponding to a row in the illustration of

the request memory 5. Since, with four modules, a maximum of four requests can be made per clock cycle, a block therefore has four cells. In the present example, the request memory 5 also has a memory depth of four.

In line with the illustration, at the time "a" (specifically during a clock cycle a), the modules 1-4 have made requests (1a, 2a, 3a, 4a), which have been stored in the four cells of the first memory block. It is then stipulated that the requests stored within a common memory block be processed in a fixed order. By way of example, the bus is thus used in the subsequent four clock cycles in succession by the modules 1, 2, 3 and finally 4.

While the request 1a was being processed, however, the modules 3 and 4 made further bus use requests (3b, 4b) in the subsequent clock cycle b, said bus use requests having been stored in the next memory block. Since the two first modules 1 and 2 did not make any requests in this clock cycle, the corresponding cells in this second block remain free.

In the next clock cycle, in which the request 2a was processed, the modules 1 to 3 finally made the requests 1c, 2c and 3c, and in the next clock cycle (processing of request 3a) the modules 2 to 4 made the requests 2d, 3d and 4d. Since the request memory 5 in the illustration has a memory depth of four blocks, each memory block is now occupied by at least one request which has not yet been processed, since it is first necessary to handle the request 4a in order to empty the first block completely. In this case, the use of the request memory 5 is identical in the arbiters in the four modules 1 to 4. This use state is communicated to the modules by their respective arbiters, so that initially no further bus requests are made. When the request 4a has also been processed, which means that the lowest memory block becomes free again, is it possible for new requests to be made. Hence, the requests result in the bus being used in the same order as the one in which they were made. It should be noted that the times a, b, c and d do not necessarily have to

be successive clock cycles, since a memory block is filled if at least one request has been made in a clock cycle.

If the arbiter A1 decides that, on the basis of the requests stored in the request memory 5, the module 1 can use the bus, it tells the module 1 via an internal grant line G1.

In a more complex bus system, some of the bus users perform more important tasks than others. To give preference to the requests from these modules, which might be a bus bridge, for example, the arbiters are allocated a further request memory 6, as shown in figure 2, which stores prioritized requests from the newly added prioritized modules 10 and 11. This additional request memory 6 operates on the basis of the same principle as the original request memory described above, i.e. the memory blocks are filled in the same way as in the conventional request memory 5. However, it may now have been stipulated that the requests stored in this additional memory 6 be handled with priority by the arbiters A1. In this case, by way of example, an arbitration algorithm can be implemented which first handles a request from the nonprioritized modules 1 to 4 and then handles two requests from the prioritized modules 10 and 11. If the two request memories 5 and 6 are used as shown in figure 2, this would result in the requests being granted in the following order: 1A, 10A, 10B, 2a, 11B, 10C, 3a, 10D, 4a, 3b, 4b, etc.

The prioritized modules 10 and 11 are also permitted to make requests until this additional use memory 6 for prioritized requests is full, irrespective of the degree of use of the original request memory 5. The request times in small and capital letters are not correlated to one another in this context.

If, finally, other priority levels for granting the bus also need to be taken into account, then a corresponding number of request memories need to be allocated to the arbiters, and the arbitration

algorithm described by way of example above needs to be of corresponding design.

Since, on the basis of the firmly prescribed decision pattern for use of the bus lines, each module itself knows when it can use the bus the next time, it can prepare for bus use, i.e. may perform other calculations in the intervening time period. In addition, each module can, if designed appropriately, make as many requests as optimize its bus use. Since, in addition, the long delay times for the grant signals which arise in the case of a central arbiter are eliminated, the bus can be operated at a higher clock rate. The inventive method thus affords the opportunity to utilize the bus and computation capacities of the system much more effectively than was previously the case.

Description

Method for interchanging data between modules connected to a common bus

The present invention relates to a method for interchanging data between modules connected to a common bus, and an apparatus for carrying out this method.

Normally, computers contain a series of hardware modules which are connected to a common bus, for example to an ISA bus or to a PCI bus. In this context, a plurality of these hardware modules - generally called bus masters - are authorized to send to the bus lines signals which can then be received by the other bus users, e.g. slaves. In this case, it is necessary to ensure that two bus masters do not send signals to the bus lines at the same time. For this reason, the bus systems normally have a central administration module (arbiter) which allocates the bus to the individual bus masters at particular times for data transmission.

If a bus master wishes to use the bus for a particular period of time, it sends the arbiter appropriate bus request information via a request line connecting the bus master to the central arbiter. In this context, one request line needs to be provided between every single bus master and the arbiter. The arbiter itself has, by way of example, a memory storing the bus requests coming from the various bus masters, and then allocates the bus to one of the bus masters for one or more clock cycles on the basis of a prescribed decision pattern. In this context, the bus is allocated by transmitting a special grant signal via an allocation or grant line, and again there needs to be one such grant line between every single bus master and the arbiter.

Since the individual bus masters respectively output data to the bus only when they have been granted permission to do so by the central arbiter, two bus masters are certain never to operate the bus, i.e. to send a signal to the bus lines, at the same time.

If the bus system is very large and highly ramified and has a very large number of bus users, then the solution just described often needs to allow for a relatively long delay time for the request and allocation information. However, this means that the bus can operate only at a relatively low clock rate and hence only slowly on the whole. Another problem is that, although the bus masters can at any time send their bus request information to the arbiter, they then need to wait for some time until they can actually use the bus. However, since they themselves do not know the exact time of bus allocation, the time between sending the bus request information and receiving the allocation information remains unused. The result of this is that the individual bus users cannot utilize their computation power to optimum effect.

It is therefore an object of the present invention to specify a method and a system for interchanging data between modules connected to a common bus where the bus lines and the computation capacities of the individual modules can be used as effectively as possible.

The object is achieved by a method having the features of claim 1 and by a system in accordance with claim 7. According to the invention, the bus system is now no longer administered by a single central administration module but rather by all the modules incorporated in the system, with each module deciding, independently of the other bus users, whether or not it sends data to the bus lines during a particular bus clock cycle. Hence, each module has a personal arbiter of its own. So that this method also ensures that the bus is not operated by two users at the same time during a

particular clock cycle, a module wishing to operate the bus first outputs bus request information which is received by all the other modules. The time of the request - that is to say the clock cycle - and the origin of the bus request information - for example a number or address for the module - are stored in a request memory which is present in all the modules (including in the request memory in that module which has itself output the bus request information), so that all the modules have the same bus request information available. On the basis of this bus request information, the modules then decide, in each case individually, whether they use the bus in a particular clock cycle, the decision being made on the basis of a prescribed decision pattern which is identical for all the modules.

Since each bus user itself decides directly whether or not it uses the bus, this method eliminates the delay time for the allocation or grant signal, which means that the bus can operate more quickly on the whole. Since all the bus users now have identical bus arbiters, i.e. arbiters which store the bus request information in the same way and make a decision about the bus use on the basis of the identical decision pattern, each bus user knows the current use status and the subsequent use status of the bus. An individual module, for example which knows that it cannot use the bus for a few clock cycles, can use the time in between for other tasks, which means that the inventive method allows more effective utilization of the individual bus users. So that the distributed arbiters can operate starting form the same basic state, they are synchronized at the start using a synchronous reset signal.

Developments of the invention are covered by the subclaims. Preferably, the decision about use of the bus is made on the basis of the decision pattern such that the bus is operated by the modules in the order in

time in which the bus request information was output. In this case, the request memories present in all the bus users are preferably in the form of a FIFO (First in, First out). Normally, however, the smallest unit of time which can still be distinguished in bus systems is a single clock cycle. It is therefore possible for a plurality of modules to output bus request information at the same time in a clock cycle. Provision can then be made for the order of bus use to be produced by a plurality of bus request information items output in a single clock cycle on the basis of a specific prescribed order.

The smallest unit of time which can still be distinguished in the bus system is a single clock cycle, as mentioned previously. The case may therefore arise in which a plurality of modules (in the extreme case all of the modules) make a request in one clock cycle, in which case only one respective module can use the actual bus lines used for transmitting signals per clock cycle, however. If, for example in a system in which a bus transfer uses the bus only for one clock cycle, all n bus users request the bus at the same time, then the entire processing or use of the bus takes n clock cycles on account of these n requests, whereas the requests were themselves output only in a single clock cycle. This in turn means that, while the n requests are being processed, the bus users can continue to make new requests, so that the request memory can become full over time. To prevent requests from being made which are no longer stored and hence can also no longer be processed, it is necessary to ensure that each module "knows" when the memory resources for new requests have been exhausted. Since the local arbiters in each module are of identical design, and hence the utilization of the memory resources is the same everywhere, each individual module can obtain or derive this information from its personal arbiter, so that it is possible to stipulate that the modules send no further requests to their

request lines until memory capacity is free again in their own arbiter.

It is also conceivable for some of the bus users to perform more important tasks for the overall system, which means that their bus requests should be handled with preference. So that it is likewise possible to allow for this, provision can be made for each bus user to have, besides the original request memory, a further request memory for requests having a higher priority level, in which the requests from these special bus users are stored separately. On the basis of the decision pattern, provision can then be made for the bus to be used on the basis of a prescribed sequence for requests from the normal request memory or for requests having the higher priority level. This second request memory is filled, and the order in time of the bus use by the prioritized requests occurs, irrespective of the processing of the normal bus requests. If further different priority levels need to be taken into account as well, then a correspondingly large number of request memories are required and the arbitration algorithm, that is to say the order in which the bus is used by requests from the various memories, needs to be adjusted as appropriate.

On the basis of another aspect of the invention, a bus system for interchanging signals between a plurality of modules is specified where each module has an outgoing request line which branches to all the other modules, and where each module has at least one request memory storing the time of bus request information and the origin thereof, and also a bus use circuit which, on the basis of the stored bus request information, permits or prevents use of the bus by the module in a particular clock cycle in line with a prescribed decision pattern which is identical for all the modules.

In this context, the term module denotes every single bus user, which can involve combined assemblies or else single IC chips, for example.

The invention is explained in more detail below with reference to the appended drawing, in which:

Figure 1 shows an illustration of the inventive linking of four bus users; and

Figure 2 shows a schematic illustration of the storage and processing of bus request information.

Figure 1 shows the connection of four modules 1-4 in an inventive bus system. It does not show the bus lines used for the actual data transfer. Each module 1-4 has a respective outgoing request line R1-R4 which branches to all the other modules, so that bus request information can be communicated to all the modules. To allow all the modules 1-4 to respond synchronously in time, they are synchronized by a common timer line C1. In addition, a reset signal can be transmitted to the modules 1-4 at the start via a reset line Re, said reset signal putting all the bus users, specifically the respective arbiters - that is to say the bus use circuits - and the content of the request memories, into a common initial state. According to the invention, any of the modules 1-4 makes a bus request for use of the bus for the duration of a transfer by activating its respective request line R1-R4 for one clock cycle. If the module wishes to request the bus for two transfers, the appropriate request line R1-R4 is activated for two clock cycles.

The filling of the request memory and the processing of the various requests will now be explained with reference to figure 2. Figure 2 shows the first module 1 in enlarged form. The arbiter A1 (the bus use circuit) responsible for use of the bus lines has in this case been permanently incorporated into the module

1. In addition, this arbiter A1 first has an associated first request memory 5, which is preferably in the form of a FIFO.

In the present example, it may first be assumed that a total of four modules are available as bus users with equal authorization. The module 1 makes a bus use request by activating its internal request line 7. This internal request line 7 is connected first directly to the request memory 5 and secondly to the external request line R1, which in turn branches to all the other modules - as shown in the present case to the second module 2.

Since the delay times for the bus request information can vary slightly depending on the length of the request lines R1-R4, only the information regarding in which clock cycle a request was made is stored in the request memory 5, but not the exact time. Within a clock cycle, each module 1-4 can make a maximum of one requests. This is covered by virtue of all the requests made within a clock cycle being stored in a memory block, corresponding to a row in the illustration of the request memory 5. Since, with four modules, a maximum of four requests can be made per clock cycle, a block therefore has four cells. In the present example, the request memory 5 also has a memory depth of four.

In line with the illustration, at the time a (specifically during a clock cycle a), all the modules 1-4 have made requests (1a, 2a, 3a, 4a), which have all been stored in the four cells of the first memory block. It is then stipulated that all the requests stored within a common memory block be processed in a fixed order. By way of example, the bus is thus used in the subsequent four clock cycles in succession by the modules 1, 2, 3 and finally 4.

While the request 1a was being processed, however, the modules 3 and 4 made further bus use requests (3b, 4b)

in the subsequent clock cycle b, said bus use requests having been stored in the next memory block. Since the two first modules 1 and 2 did not make any requests in this clock cycle, the corresponding cells in this second block remain free.

In the next clock cycle, in which the request 2a was processed, the modules 1 to 3 finally made the requests 1c, 2c and 3c, and in the next clock cycle (processing of request 3a) the modules 2 to 4 made the requests 2d, 3d and 4d. Since the request memory 5 in the illustration has a memory depth of only four blocks, each memory block is now occupied by at least one request which has not yet been processed, since it is first necessary to handle the request 4a in order to empty the first block completely. In this case, the use of the request memory 5 is identical in all the arbiters in the four modules 1 to 4. This use state is communicated to the modules by their respective arbiters, so that initially no further bus requests are made. Only when the request 4a has also been processed, which means that the lowest memory block becomes free again, is it possible for new requests to be made. Hence, all the requests result in the bus being used in the same order as the one in which they were made. It should be noted that the times a, b, c and d do not necessarily have to be successive clock cycles, since a memory block is filled only if at least one request has been made in a clock cycle.

If the arbiter A1 decides that, on the basis of the requests stored in the request memory 5, the module 1 can use the bus, it tells the module 1 via an internal grant line G1.

In a more complex bus system, some of the bus users normally perform more important tasks than others. To give preference to the requests from these modules, which might be a bus bridge, for example, the arbiters are allocated a further request memory 6, as shown in

figure 2, which stores only prioritized requests from the newly added prioritized modules 10 and 11. This additional request memory 6 operates on the basis of the same principle as the original request memory described above, i.e. the memory blocks are filled in the same way as in the conventional request memory 5. However, it may now have been stipulated that the requests stored in this additional memory 6 be handled with priority by the arbiters A1. In this case, by way of example, an arbitration algorithm can be implemented which first handles a request from the nonprioritized modules 1 to 4 and then handles two requests from the prioritized modules 10 and 11. If the two request memories 5 and 6 are used as shown in figure 2, this would result in the requests being granted in the following order: 1A, 10A, 10B, 2a, 11B, 10C, 3a, 10D, 4a, 3b, 4b, etc.

The prioritized modules 10 and 11 are also permitted to make requests only until this additional use memory 6 for prioritized requests is full, irrespective of the degree of use of the original request memory 5. The request times in small and capital letters are not correlated to one another in this context.

If, finally, other priority levels for granting the bus also need to be taken into account, then a corresponding number of request memories need to be allocated to the arbiters, and the arbitration algorithm described by way of example above needs to be of corresponding design.

Since, on the basis of the firmly prescribed decision pattern for use of the bus lines, each module itself knows when it can use the bus the next time, it can prepare for bus use, i.e. may perform other calculations in the intervening time period. In addition, each module can, if designed appropriately, make as many requests as optimize its bus use. Since, in addition, the long delay times for the grant signals

which arise in the case of a central arbiter are eliminated, the bus can be operated at a higher clock rate. The inventive method thus affords the opportunity to utilize the bus and computation capacities of the system much more effectively than was previously the case.

Patent Claims

1. A method for interchanging data between modules (1-4) connected to a common bus, having the following steps:
all the modules (1-4) are synchronized in time;
a module (1-4) wishing to operate the bus outputs bus request information which is received by the other modules (1-4);
all the modules (1-4) store the clock cycle of the output and the origin of the bus request information in a request memory (5);
each module (1-4) uses the stored bus request information (1a, 2a, 10A, 10B) to decide, independently of the other modules (1-4), whether there is a signal on the bus in a particular clock cycle, the decision being made on the basis of a prescribed decision pattern which is identical for all the modules (1-4).

2. The method as claimed in claim 1,
characterized
in that, at the start of the method, all the request memories (5) are put into an identical initial state by a reset signal.

3. The method as claimed in claim 1 or 2,
characterized
in that, on the basis of the decision pattern, the bus is operated by the modules (1-4) in the order in time in which the corresponding bus request information was output.

4. The method as claimed in claim 3,
characterized
in that, if a plurality of modules (1-4) output bus request information at the same time in a clock cycle, the corresponding information is stored in a shared

memory block in the request memory (5), and, in accordance with the decision pattern, the bus is used in a prescribed order on the basis of information (1a, 2a, 3a, 4a) stored in a memory block.

5. The method as claimed in claim 4,
characterized
in that the modules (1-4) output no further bus request information if the number of the at least partly used memory blocks has reached a prescribed limit value.

6. The method as claimed in one of the preceding claims,
characterized
in that some modules can output bus request information having a higher priority level, where
the appropriate information (10A, 10B) is stored in a further memory (6),
the bus is used on the basis of a prescribed use algorithm for bus request information in the first use memory (5) or for bus request information having the higher priority level in the further memory (6), and
the bus is used on the basis of the bus request information having the higher priority level irrespective of use on the basis of the normal bus request information.

7. A system for interchanging data between modules (1-4) connected to a common bus, having:
request lines (R1-R4), which respectively connect one module (1-4) to the other modules (1-4), for transmitting bus request information;
a request memory (5) in each of the modules (1-4) for storing the clock cycle of the output and the origin of the bus request information;
a bus use circuit (A1) in each of the modules (1-4) for controlling bus use by the appropriate module (1-4) on the basis of the bus request information (1a, 2a, 10A,

10B) stored in the request memory (5) in line with a decision pattern which is prescribed and identical for all the modules (1-4); and
a timer line (C1), connected to all the modules (1-4), for synchronizing the modules (1-4).

8. The system as claimed in claim 7,
characterized
in that the system also has a line (Re) for transmitting a reset signal which puts all the request memories (5) into a standard initial state.

9. The system as claimed in claim 7 or 8,
characterized
in that each module (1-4) has a further memory (6) for higher priority bus request information which is output by some modules, where the bus use circuits (A1) take into account the higher priority bus request information stored in this further memory (6) on the basis of a prescribed use algorithm.

Abstract

Method for interchanging data between modules connected to a common bus

In a method for interchanging data between modules (1-4) connected to a common bus, all the modules (1-4) are synchronized. A module (1-4) wishing to operate the bus outputs bus request information which is received and stored by the modules (1-4). Each module (1-4) uses the stored bus request information (1a, 2a, 10A, 10B) to decide, independently of the others, whether there is a signal on the bus in a particular clock cycle, the decision being made on the basis of a prescribed decision pattern which is identical for all the modules (1-4).

[Figure 2]

Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

As a below named inventor, I hereby declare that:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

My residence, post office address and citizenship are as stated below next to my name,

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I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Verfahren zum Austausch von Daten zwischen an einen gemeinsamen Bus angeschlossenen Modulen

Method for exchanging data between modules connected to a common bus

deren Beschreibung

the specification of which

(zutreffendes ankreuzen)
☐ hier beigefügt ist.
☒ am 06.09.2000 als
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Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

German Language Declaration

Prior foreign appplications
Priorität beansprucht

			Priority Claimed	
19942676.7	DE	07.09.1999	☒	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
Text22□Text23	FORMTEXT	Text23 Franz	Hutner	Franz
(Number)	(Country)	(Day Month Year Filed)	☐ Yes	☐ No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein
(Number)	(Country)	(Day Month Year Filed)	☐ Yes	☐ No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

PCT/DE00/03086	06.09.2000	anhängig	pending
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D, M, Y) (Anmeldedatum T, M, J)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
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(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M; J)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

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German Language Declaration

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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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Unterschrift des Erfinders Datum	Inventor's signature Date
Franz Hutner 6.2.2002	Franz Hutner 6.2.2002
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Staatsangehörigkeit	Citizenship
DE	DE
Postanschrift	Post Office Addess
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Unterschrift des Erfinders Datum	Second Inventor's signature Date
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Wohnsitz	Residence
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(Supply similar information and signature for third and subsequent joint inventors).